## REMARKS

### *In the Specification*

With respect to Detailed Action Item 3:

The specification has been objected to as failing to provide proper antecedent basis for the claimed subject matter. The explanation in the Office Action provides:

> "Claims 2 and 20 state that the cache coherency protocol of claims 1 and 18 interfaces with the storage controller. However, the cache coherency protocol is self-contained within the bounds of the instruction and data caches of the central processing unit and is merely a statement of policy. It is unclear from the specification how this protocol interfaces with the storage controller because interfacing implies communication between independent entities, whereas the policy statements comprising the protocol do not provide a means for such communication."
>
> "Claims 3, 4, 21 and 23 state that the cache coherency protocol of claims 1 and 18 interfaces with existing cache handling requirements. Again, it is unclear from the specification how the policy statements comprising the protocol of claims 1 and 18 interface with the cache handling requirements, which likewise are merely statements of necessary conditions and do not provide a means for the communication implied by interfacing."
>
> "For the purposes of examination, claims 2 and 20 will be interpreted to teach that the cache coherency protocol of claims 1 and 18 is combined with the processor system cache coherency protocol employed by the storage controller."
>
> "Claims 3, 4, 21 and 23 will be interpreted to teach that the cache coherency protocol of claims 1 and 18 is combined with existing cache handling requirements."

Applicants respectfully submit that the specification is adequate in that it teaches that the cache coherence protocol of the processor interfaces with that of the storage controller and the implementation employing a status indicator to facilitate the interface between the two protocols. Reference may be made to page 2, line 26 and page 4 line 17. Applicants respectfully disagree with the Examiner's assertion as to interpretation of the claims. The cache coherency protocol of claims 1 and 18 is not the same or combined with the processor system cache coherency protocol employed by the storage controller.

Similarly, that the cache coherency protocol of claims 1 and 18 is not the same or combined with existing cache handling requirements, but operates in cooperation with them.

***Claim Objections***

With respect to Detailed Action Item 3:

> Claims 1-17 and 19-35 are objected to because of the following informalities:
>
> The term "access" (Claim 1, lines 8,10 and 12; claim 13, line 1; claim 19, lines 2,4 and 7; claim 31, line 1) suggests both reading and writing and is therefore inconsistent with the specification, in which only exclusive status is associated with read and write capability (Page 5, lines 6-10).
>
> In order to be consistent with the specification, it is suggested that the term "access" in line 8 of claim 1, line 1 of claim 13, line 2 of claim 19, and line 1 of claim 31 be replaced with "read access" and the term "access" in line 12 of claim 1 and 7 of claim 19 be replaced with "write access". For clarity, it is suggested that the first instance of the term "access" in line 10 of claim 1 and line 4 of claim 19 be replaced with "read and write access". The claim(s) will be interpreted in light of this suggestion.

Applicants appreciate the Examiner's suggestion and respectfully submit that the suggested amendment is not required, but merely provides additional clarification. To that end, Applicants have amended the Claims 1, 13, 19, and 31 in accordance with the Examiner's suggestions to provide clarification and facilitate prosecution.

> The specification defines distinct cache-block statuses among the instruction and data cache (Page 5, lines 15-16 and 20-21). It is unclear in claim 1, lines 9,11 and 13 and claim 19, lines 3,5 and 8 to which cache the status applies. It is suggested that the phrase "in the instruction cache and the operand cache" be inserted after "read only status" in line 9 of claim 1 and line 3 of claim 19. It is also suggested that the phrase "in the operand cache" be inserted after "exclusive status" in lines 11 and 13 of claim 1 and lines 5 and 8 of claim 19. The claim(s) will be interpreted in light of this

suggestion.

Applicants once again appreciate the Examiner's suggestion and respectfully submit that the suggested amendment is not required, but merely provides additional clarification. To that end, Applicants have amended Claims 1 and 19 in accordance with the Examiner's suggestions to provide clarification and facilitate prosecution.

> The phrase "if said cache block has already been accessed by said instruction cache" (Claim 1, line 13; claim 19, lines 8-9) is not consistent with the specification. It is presumed that this phrase is meant to suggest that the cache block has read-only status in the instruction cache. However, merely having been accessed at some time in the past does not require that the block has read-only status as the status may have changed in the intervening time. It is suggested that this phrase be replaced by the phrase "if said cache block has read-only status in the instruction cache". The claim(s) will be interpreted in light of this suggestion.

Applicants once again appreciate the Examiner's suggestion have amended the Claims 1 and 19 in accordance with the Examiner's suggestions to provide the clarification.

> The phrases "buffering a register of cache locations" and "for fetched unexecuted instructions" (Claim 5, lines 2-3; claim 24, lines 2-3) are unclear and do not reflect the specification (Page 5, lines 17-24). It is suggested that these phrases be replaced by the phrases "buffering cache block addresses in a register-file" and "corresponding to fetched unexecuted instructions", respectively. The claim(s) will be interpreted in light of this suggestion.

Applicants once again appreciate the Examiner's suggestion and respectfully submit that the suggested amendment is not required, but merely provides additional clarification. However, Applicants have amended Claims 5 and 24 in accordance with the Examiner's suggestions to provide clarification and facilitate prosecution.

In lines 10-11 of claim 5 and lines 10-11 of claim 24, the phrase "said associated cache block" is improper because an associated cache block has not been previously recited in the claims. It is presumed that the cache block being referred to is that found in line 4 of the claims. It is suggested that the phrase "a cache block's status" (Claim 5, lines 4-5; claim 24, lines 4-5) be replaced by the phrase "an associated cache block's status". The claim(s) will be interpreted in light of this suggestion.

Applicants once again appreciate the Examiner's suggestion and respectfully submit that the suggested amendment is not required. In this instance, the suggested amendment would change the meaning of the claim. The cache block is one in instruction cache that corresponds to the desired storage address in operand cache. Therefore, the amendment required it to change "said associated cache block" to "an associated cache block." Applicants have amended Claims 5 and 24 accordingly.

Claims 7 and 26 recite "said request" (Claim 7, lines 2 and 4; claim 26, lines 2 and 4), referring to the request for exclusive status found in lines 5-6 of claims 5 and 24. This may be confused with the requested fetch found in line 12 of claims 5 and 24, respectively. For clarity, it is suggested that this phrase be replaced by the phrase "said request for exclusive status". The claim(s) will be interpreted in light of this suggestion.

Applicants once again appreciate the Examiner's suggestion have amended Claims 7 and 26 accordingly to provide clarification.

The phrase "said probe and" (Claim 8, line 3; claim 27, line 3) " is improper because a probe has not been previously recited in the claims. It is suggested that this phrase be deleted. The claim(s) will be interpreted in light of this suggestion.

Applicants once again appreciate the Examiner's suggestion have amended Claims 8 and 27 accordingly to provide clarification.

The term "I-cache" (Claim 11, line 2; claim 29, line 2) " is improper because an I-cache has not been previously recited in the claims. It is suggested that this term be replaced with "instruction cache". The claim(s) will be interpreted in light of this suggestion.

Applicants once again appreciate the Examiner's suggestion have amended Claims 11 and 29 accordingly to provide clarification.

Claims 17 and 35 recite a "said processor system cache coherency protocol" (Claim 17, lines 1-2; claim 35, lines 1-2), however there is no instance of a processor system cache coherency protocol in the parent claims 16 and 34. However, claims 2 and 20 recite this limitation. It is suggested that claims 16 and 34 be modified to reference claims 2 and 20, respectively. The claim(s) will be interpreted in light of this suggestion.

Applicants once again appreciate the Examiner's suggestion have amended Claims 16 and 34 accordingly to provide clarification.

Claim 20 contains a typographical error. A redundant instance of the word "includes" appears in line 2. It is suggested that this instance be deleted. The claim(s) will be interpreted in light of this suggestion.

Applicants once again appreciate the Examiner's suggestion have amended Claims 7 and 26 accordingly to provide clarification.

***Claim Disposition***

Claims 1-35 are pending in the application. Claims 1 – 7, 9 – 26, and 28 – 35 have been rejected. Claims 8 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims, following correction of all other outstanding objections.

***Claim Rejections 35 U.S.C. §102(b)***

Claims 1-4 and 13-17 stand rejected under 35 U.S.C. 102(b) as being anticipated by Anderson, U.S. Patent No. 3,735,360, hereinafter Anderson. The Examiner states that Anderson teaches:

> "As in claims 1-4 and 13-17, Anderson describes a multi-processor system comprising a pair of parallel and independent caches subjected to a cache coherency protocol and sharing a common main storage (Fig. 1, elements 10, 15 and 16; column 5, lines 18-26), where a cache can have the only copy of a block of data (i.e. exclusive) or one of multiple copies of a block of data (i.e. shared), indicated by a fetch-only bit (Fig. 3, element 62; column 8, lines 10-2 1) in the cache directory (Fig. 3, element 27; column 5, lines 46-49).
>
> "Anderson further describes that when the block of data has exclusive status in a cache, the block may be stored into (i.e. written), but when the block of data is shared it may only be read (Column 8, lines 22-35). This latter state corresponds to a read-only status. Anderson further emphasizes that before a block of data can be stored into, other existing copies must be invalidated and exclusive ownership must be obtained (Column 8, lines 35-39)."
>
> "Therefore, the protocol described by Anderson may be summarized as:
>
> allowing shared read access by a first cache and second cache to a cache block if the cache block has read-only status in the first cache and the second cache;
>
> allowing read and write access by the first cache and preventing access by the second cache to the cache block if the cache block has exclusive status in the first cache; and
>
> interlocking write access to the cache block by the first cache with exclusive status if the cache block has read-only status in the second cache;

where the first and second caches may be equated with the operand and instruction cache, respectively."

"As in claims 2-4 and 16-17, Anderson combines the above cache coherency protocol with existing cache handling requirements and a processor system cache coherency protocol, both employed by a storage control unit, and allowing shared access to cache blocks among a plurality of central processing units (Fig. 1, elements 21,22 and 29-32; column 3, line 64 to column 5, line 8; column 4, line 52 to column 5, line 2, column 5, line 34 to column 6, line 4)."

Applicant respectfully contends that the explanation in the Office Action significantly mischaracterizes the teachings of Anderson and ignores several limitations of the claim. To anticipate a claim under 35 U.S.C. §102, a single source must contain all of the elements of the claim. *Lewmar Marine Inc. v. Barient, Inc.*, 827 F.2d 744, 747, 3 U.S.P.Q.2d 1766, 1768 (Fed. Cir. 1987), cert. denied, 484 U.S. 1007 (1988). Moreover, the single source must disclose all of the claimed elements "arranged as in the claim." *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 716, 223 U.S.P.Q. 1264, 1271 (Fed. Cir. 1984). Missing elements may not be supplied by the knowledge of one skilled in the art or the disclosure of another reference. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 780, 227 U.S.P.Q. 773, 777 (Fed. Cir. 1985).

With regard to Claim 1, Applicant respectfully contends that Anderson does not teach or disclose each element of the invention "arranged as in the claim". Specifically, Anderson does not teach or disclose, "A method of supporting programs that include instructions **that modify subsequent instructions** in a processor system with a storage controller and a central processing unit including an execution unit, an instruction unit, and a plurality of caches **including separate instruction cache and operand cache**". Applicants respectfully submit that the Examiner has significantly mischaracterized the claims by giving them an overly broad interpretation. In particular, completely ignoring the wording of the preamble that specifies the realm of the art and the improvement thereto. Simply put, Applicants are not suggesting that the concept of a cache coherency

protocol is novel, in fact, the present invention acknowledges as much and specifically claims interfacing with and existing cache coherency protocol. Moreover, Anderson does not teach or disclose a separate instruction and operand caches, nor the difficulties overcome by the present invention to implement a cache coherency protocol therewith. Anderson merely addresses the ability to share data between two processors. It is appreciated that Anderson is drawn to an interlocking scheme which permits multiprocessing in a shared storage configuration,. Logically, Anderson teaches and discloses similar processes. However, Anderson does not teach or disclose anything with respect to a plurality of caches **including separate instruction cache and operand cache**. Therefore, because Anderson does not teach or discloses each element of the claimed invention, it cannot anticipate Applicants' claims. Thus, Claim 1 is allowable, the rejection is improper, and it should be withdrawn.

Moreover, with regard to Claims 2 – 4, and 13 - 17, these claims include the abovementioned limitations and based on the arguments above are therefore, also allowable. Thus, Claims 2 – 4, and 13 - 17 are allowable and the rejections should be withdrawn. Additionally, Claims 2 – 4, and 13 – 17 depend from Claim 1 directly or indirectly, an allowable claim based upon the abovementioned reasoning, and therefore because these claims depend from a claim that is allowable, they too are allowable and the rejections should be withdrawn. MPEP 2143.03.

Claims 18 and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaskins U.S. Patent No. 5,930,821, hereinafter Gaskins. The Examiner states that Gaskins teaches:

> "As in claims 18 and 34-35, Gaskins discloses a system supporting self-modifying code in a processor system (Column 9, lines 19-24) comprising:
>
> a storage controller (Fig. 6, elements 620, 640 and 642); and
>
> a central processing unit (Fig. 6, element 602) including an execution unit (Fig. 6, element 624), an instruction unit (Fig. 6, element

622), and a plurality of caches including a separate instruction cache and operand cache (Fig. 6, elements 605 and 607);

where it is noted that the storage controller function is shown distributed among three elements (Fig. 6, elements 620, 640 and 642) integrated within the central processing unit, yet it may still be interpreted from Fig. 6 of Gaskins that the system further comprises:

the central processing unit coupled to the storage controller;

the execution unit coupled to the instruction unit, the instruction cache and the operand cache;

the instruction unit coupled to the instruction cache and the operand cache; and the instruction cache coupled to the operand cache."

"As in claims 18 and 34-35, Gaskins describes the above system further subjecting the instruction cache and operand cache of the central processing unit to a cache coherency protocol with interlocks on cache block access (Column 3, lines 50-53; Figs. 7 and 8; column 7, lines 60-62; column 8, lines 56-58)."

"As in claim 34, the processor system of Gaskins includes a plurality of Bus Masters (Fig. 2, elements 110, 112 and 114) that share access to the main memory and level-2 cache (Fig. 2, elements 106 and 108), where it is readily apparent that Bus Masters may include a central processing unit."

"As in claim 35, the processor system cache coherency protocol of Gaskins allows the central processing unit to share access to cache blocks with other Bus Masters (Fig. 2, elements 106 and 108, column 2, lines 15-17 and 48-65), where it is readily apparent that Bus Masters may include a central processing unit."

With regard to Claim 18, Applicant respectfully contends that Gaskins does not teach or disclose each element of the invention "arranged as in the claim". Specifically, Gaskins does not teach or disclose, "a storage controller", or "said central processing unit coupled to said storage controller". Applicants respectfully submit, that the Examiner suggests that the storage controller is internal to the CPU and comprised of the three elements of 620, 640, and 642, this clearly is not equivalent to the claim terminology.

First, it is apparent from the wording of the claim, figures, and specification, that the storage controller is external to the CPU (and provides for interfaces with other CPU's). To read the language of the claim in any other fashion would be to distort the meaning of the wording. For example, were the storage controller meant to be part of the CPU, it would have been claimed as included with the CPU as the execution unit, instruction unit, instruction cache and operand cache were. Second, the approach suggested by the Examiner clearly mischaracterizes Gaskins, and clearly does not teach or disclose the elements of the invention "arranged as in the claim" as required by *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 716, 223 U.S.P.Q. 1264, 1271 (Fed. Cir. 1984). Therefore, Gaskins does not teach or disclose an element of the claimed invention.

Moreover, Gaskins does not teach or disclose, "said execution unit coupled to said instruction unit, or said instruction cache and said operand cache". Note from figure 6 as cited by the Examiner, there is no disclosure or teaching showing the ALU 624 coupled with the code cache 605, nor the data cache 607. In addition, Gaskins does not teach or disclose "said instruction unit coupled to ... and said operand cache". Note from figure 6 as cited by the Examiner, there is no disclosure or teaching showing the control unit 622 coupled to the data cache 607. Therefore, once again, Gaskins does not teach or disclose an element of the claimed invention. Because Gaskins does not teach or discloses each element of the claimed invention, it cannot anticipate Applicants' claims. Thus, Claim 18 is allowable, the rejection is improper, and it should be withdrawn.

Moreover, with regard to Claims 19 – 35, these claims include the abovementioned limitations and based on the arguments above are therefore, also allowable. Thus, Claims 19 - 35 are allowable and the rejections should be withdrawn. Additionally, Claims 19 - 35 depend from Claims 18, which is allowable based upon the abovementioned reasoning, and therefore because these claims depend from a claim that is allowable, they too are allowable and the rejections should be withdrawn. MPEP 2143.03.

With regard to Claims 34 - 35, Applicant respectfully contends that Gaskins does not teach or disclose each element of the invention "arranged as in the claim". Specifically, Gaskins does not teach or disclose, "a multi-processor system including a

plurality of central processing units", or "said processor system cache coherency protocol is an existing protocol that allows said central processor to share access to cache blocks with other central processing units of said plurality of central processing units in said processor system." Applicants respectfully submit, that the Examiner suggests that the bus master 110 "*may* include a CPU". Applicants note that there is no specific teaching in Gaskins that the bus masters do in fact include a CPU, moreover that any form of a processor system cache coherency protocol is disclosed. All that Gaskins provides for teaching with regard to the bus masters 110 -- 114 is that "performance of the computer system 100 is improved because other devices such as the bus master devices 110-114, can utilize the system bus 116 while the microprocessor 102 is executing instructions. Clearly this disclosure is descriptive of a bus sharing protocol not a cache coherence protocol. Therefore, because does not teach or disclose an element of the claimed invention, it cannot anticipate Applicants' claims. Thus, Claims 34 - 35 are allowable, the rejections are improper, and they should be withdrawn.

***Claim Rejections 35 U.S.C. §103(a)***

Claims 5-7, 9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. Patent No. 3,735,360), hereinafter Anderson, in view of Mahalingaiah et al. (U.S. Patent No. 6,073,217), hereinafter Mahalingaiah, and Gaskins (U.S. Patent No. 5,930,821), hereinafter Gaskins. The Examiner states:

> "Anderson is relied upon for the teachings relative to claim 3 as above."
>
> "As in claims 5-7, 9 and 11-12, Anderson also teaches that when data is required to be stored or updated, an associated cache block's status is evaluated for a desired storage address in a first cache (Fig. 2; column 8, line 55 to column 9, line 3) and a request for exclusive status is transmitted to the storage control unit and a cross-interrogate signal is transmitted to a second cache (Fig. 2; column 9, lines 4-19)."
>
> "The rationale derived from Anderson in the rejection of claim 3 above is incorporated herein for the teaching of storing in the first cache after exclusive status is obtained via the storage control unit following a

response from the cross interrogation."

"As in the rejection of claim 3 above, the first and second caches are equated to the operand and instruction cache."

"Anderson does not teach the following steps as required by claims 5-7, 9 and 11-12, however, these steps are taught by Mahalingaiah:

buffering cache block addresses in a register-file (Fig. 2, element 48) in an instruction cache (Figs. 1 and 2, element 22) corresponding to fetched unexecuted instructions in an instruction buffer in the instruction unit (Column 3, lines 1-7; column 8, lines 34-37);

discarding and refetching data in the instruction cache if the associated cache block in the instruction cache matches the desired storage address (Column 3, lines 8-12; column 8, lines 41-59);

discarding and refetching data in the instruction buffer and re-buffering cache locations in the register if an instruction stream of an execution unit (Fig. 1, element 28) changes (i.e. if the code is self-modified, see Instant Application, page 6, lines 22-24) (Column 5, lines 13-29 and 54-58; column 8, lines 41-59; column 9, lines 48-60); and

discarding data in the instruction buffer and discarding the cache locations in the register if the execution unit completes execution of fetched instructions (Column 4, lines 13-15: column 8, lines 41-59)."

"Mahalingaiah teaches that the above steps allow correct execution of self-modifying code (Column 3, lines 12-14; column 5, lines 54-58)."

"Regarding claims 5-7, 9 and 11-12, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the teachings of Mahalingaiah enumerated above, in the method of Anderson, in order to allow correct execution of self-modifying code as taught by Mahalingaiah."

"The combination of Anderson and Mahalingaiah does not teach the following step as required by claims 5-7, 9 and 11-12, however, it is taught by Gaskins:

when instruction fetch is requested, providing the instruction cache read-only status for a requested cache block (Fig. 2, element 205; column 2, lines 18-20; Fig. 8; column 8, lines 58-61)."

"It is readily apparent from Gaskins that the status for a block in the instruction cache must be read-only because the control unit (i.e. instruction unit) (Fig. 2, element 222) may only fetch instructions and maintains them prior to execution (Column 2, lines 18-27)."

"Further regarding claims 5-7, 9 and 11-12, it would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to include the teaching of Gaskins enumerated above, in the method made obvious by the combination of Anderson and Mahalingaiah, because the instruction unit may only fetch instructions."

"As in claim 7, Anderson teaches that when exclusive ownership of a cache block is requested, all other copies whether exclusive or read-only are invalidated (Column 8, lines 35-39; column 9, lines 20-32)."

"As in claims 11-12, Anderson teaches that the cross-interrogation of the cache block address is accomplished via a directory lookup in the storage control unit (Fig. 1, elements 27-28; column 4, lines 20-27 and 56-62; column 5, lines 45-48)."

"Regarding claim 12, although the combination of Anderson, Mahalingaiah and Gaskin does not teach that the cache directory and register-file comprise six locations, such limitations are merely a matter of design choice and would have been obvious in the method of Anderson, Mahalingaiah and Gaskin. The combination of Anderson, Mahalingaiah and Gaskin teaches both a directory and register file. The limitations in claim 12 of the instant application do not define a patentably distinct invention since both are directed toward providing storage for indexing cache contents and instruction fetch unit contents. The number of locations is inconsequential for the invention as a whole and presents no new or unexpected result. Therefore, to use six locations would have been an obvious design choice to one of ordinary skill in the art at the time of invention by applicant."

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing a *prima facie* case of obviousness. *In re Fine*, U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). The Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996).

With regard to Claims 5-7, 9 and 11-12, Applicants respectfully contends that neither Anderson, nor Mahalingaiah, nor Gaskins, whether alone or in combination, teach or disclose each element of the invention as discussed above. Specifically, neither Anderson, nor Mahalingaiah, nor Gaskins. teach or disclose, "A method of supporting programs that include instructions **that modify subsequent instructions** in a processor system with a storage controller and a central processing unit including an execution unit, an instruction unit, and a plurality of caches **including separate instruction cache and operand cache**" as presented above. Therefore, because neither Anderson, nor Mahalingaiah, nor Gaskins disclose or teach an element of the invention they cannot render the Applicants' claims unpatentable. Thus, Claims 5-7, 9 and 11-12 are allowable, the rejections are improper, and they should be withdrawn.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. Patent No. 3,735,360), hereinafter Anderson, in view of Mahalingaiah et al. (U.S. Patent No. 6,073,217), hereinafter Mahalingaiah, and Gaskins (U.S. Patent No. 5.930,821), hereinafter Gaskins. as applied to claim 5 above, and further in view of Handy (The Cache Memory Book, Jim Handy, 1998). The Examiner states:

> "Anderson, Mahalingaiah and Gaskins are relied upon for the teachings relative to claim 5 as above."
>
> "Anderson further teaches an existing cache handling requirement whereby entries in the cache are replaced according to a replacement algorithm (Column 9, lines 33-3 9)."
>
> "Anderson does not teach that the replacement algorithm is a least-recently used replacement algorithm as required by claim 10."
>
> "Handy teaches a least recently used cache block replacement algorithm used to determine where to place new blocks of data in a cache (Page 57, paragraph 2)."
>
> "It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the least recently used replacement algorithm taught by Handy in the method taught by the combination of Anderson, Mahalingaiah and Gaskin, for the purpose of determining where to place new blocks of data in the cache as taught by Handy."

With regard to Claim 10, Applicants respectfully contends that neither Anderson, nor Mahalingaiah, nor Gaskins, whether alone or in combination, teach or disclose each element of the invention as discussed above. Therefore, because neither Anderson, nor Mahalingaiah, nor Gaskins disclose or teach an element of the invention they cannot render the Applicants' claims unpatentable. Thus, Claim 10 is allowable, the rejection is improper, and it should be withdrawn.

Claims 19-21, 23, and 31-33 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gaskins (U.S. Patent No. 5,930,821) hereinafter Gaskins as applied to claim 18 above, and in further view of Anderson (U.S. Patent No. 3,735,360), hereinafter Anderson.

> "Gaskins is relied upon for the teachings relative to claim 18 as above."
>
> "Gaskins does not teach the limitations of claims 19-21, and 23 that require the cache coherency protocol to comprise:
>
> the storage controller allowing shared read access by the instruction cache and the operand cache to a cache block if the cache block has read-only status in the instruction and operand caches;
>
> the storage controller allowing read and write access by the operand cache and preventing access by the instruction cache to the cache block if the cache block has exclusive status in the operand cache; and
>
> the storage controller interlocking write access to the cache block by the operand cache with exclusive status if the cache block has read-only status in the instruction cache."
>
> "The rationale derived from Anderson in the rejection of claim 1 above is incorporated herein for the teaching of the above cache coherency protocol."
>
> "Gaskins also does not teach that shared read access implies that both caches may read a target cache block, that exclusive status dictates sole update access to a target cache block, and that read-only status dictates that a cache block may not be held with exclusive status as required by claims

31-33."

"The rationale derived from Anderson in the rejection of claims 13-15 above is incorporated herein for the teaching of the above limitations required by claims 31-33. It is noted that these limitations are a part of the above cache coherency protocol."

"Anderson also teaches that the cache coherency protocol (i.e. interlocking mechanism) ensures that a processor accesses the most current data (Column 3, lines 37-44)."

"Regarding claims 19-21, 23 and 31-33, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the cache coherency protocol enumerated above and taught by Anderson, in the system of Gaskins in order to ensure that a processor accesses the most current data as taught by Anderson."

"As in claims 20-21 and 23, Gaskins teaches that the cache coherency protocol is combined with existing cache handling requirements and a processor system cache coherency protocol employed by the storage controller (Column 2, lines 15-17 and 48-65), where it is noted that element 220 in Fig. 2 and element 320 in Fig. 3 both perform the same function as element 620 in Fig. 6."

With regard to Claims 19-21, 23, and 31-33, Applicants respectfully contends that neither Gaskins nor Anderson, whether alone or in combination, teach or disclose each element of the invention as discussed above with respect to Claim 18. Specifically, neither Gaskins nor Anderson, teach or disclose, "a storage controller", or "said central processing unit coupled to said storage controller". Applicants respectfully submit, that the Examiner suggests that the storage controller is internal to the CPU and comprised of the three elements of 620, 640, and 642, this clearly is not equivalent to the claim terminology as presented above. Moreover, neither Gaskins nor Anderson teach or disclose, "a processor system with a storage controller and a central processing unit including an execution unit, an instruction unit, and a plurality of caches **including separate instruction cache and operand cache**". Therefore, because neither Gaskins nor Anderson disclose or teach an element of the invention they cannot render the Applicants' claims unpatentable. Thus, Claims 19-21, 23, and 31-33 are allowable, the rejections are improper, and they should be withdrawn.

Moreover, with regard to Claims 19 – 35, these claims include the abovementioned limitations and based on the arguments above are therefore, also allowable. Thus, Claims 19 - 35 are allowable and the rejections should be withdrawn. Additionally, Claims 19 - 35 depend from Claims 18, which is allowable based upon the abovementioned reasoning, and therefore because these claims depend from a claim that is allowable, they too are allowable and the rejections should be withdrawn. MPEP 2143.03.

Claim 22 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gaskins (U.S. Patent No. 5.930,821) hereinafter Gaskins in view of Anderson (U.S. Patent No. 3,735,360), hereinafter Anderson as applied to claim 21 above, and further in view of Handy (The Cache Memory Book, Jim Handy, 1998). The Examiner states:

> "Gaskins and Anderson are relied upon for the teachings relative to claim 21 as above."
>
> "Gaskin and Anderson do not teach that the existing cache handling requirements utilize a least-recently used replacement algorithm as required by claim 22."
>
> "Handy teaches a cache handling requirement using a least recently used cache block replacement algorithm for determining where to place new blocks of data in a cache (Page 57, paragraph 2)."
>
> "It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the least recently used replacement algorithm taught by Handy in the system made obvious by the combination of Gaskins and Anderson, for the purpose of determining where to place new blocks of data in the cache as taught by Handy."

With regard to Claim 22, Applicants respectfully contends that neither Gaskins nor Anderson, nor Handy whether alone or in combination, teach or disclose each element of the invention as discussed above. Specifically, neither Gaskins nor Anderson, teach or disclose, "a storage controller", or "said central processing unit coupled to said storage controller". Applicants respectfully submit, that the Examiner suggests that the storage controller is internal to the CPU and comprised of the three elements of 620, 640, and 642, this clearly is not equivalent to the claim terminology as presented above. Moreover,

neither Gaskins, nor Anderson, nor Handy teach or disclose, "a processor system with a storage controller and a central processing unit including an execution unit, an instruction unit, and a plurality of caches **including separate instruction cache and operand cache**" as discussed above. Therefore, because neither Gaskins nor Anderson, nor Handy disclose or teach an element of the invention they cannot render the Applicants' claims unpatentable. Thus, Claim 22 is allowable, the rejection is improper, and it should be withdrawn.

Claims 24-26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaskins (U.S. Patent No. 5,930,821) hereinafter Gaskins in view of Anderson (U.S. Patent No. 3,735,360), hereinafter Anderson, and further in view of Handy (The Cache Memory Book, Jim Handy, 1998) as applied to claim 22 above, and further in view of Mahalingaiah et al. (U.S. Patent No. 6,073,217), hereinafter Mahalingaiah. The Examiner states:

> "Gaskins, Anderson and Handy are relied upon for the teachings relative to claim 22 above."
>
> "Gaskins, Anderson and Handy as applied to claim 22 above, do not teach any of the dependent limitations recited in claims 24-26 and 28-30."
>
> "The rationale derived from Gaskins in the rejection of claims 5-7, 9 and 11-12 above is incorporated herein for the following teaching required by claims 24-26 and 28-30:
>
> when an instruction fetch is requested, providing the instruction cache read-only status for a requested cache block."
>
> "The rationale derived from Anderson in the rejection of claims 5-7, 9 and 11-12 above is incorporated herein for the following teachings required by claims 24-26 and 28-30:
>
> when data is required to be stored or updated, an associated cache block's status is evaluated for a desired storage address in the operand cache and a request for exclusive status is transmitted to the storage controller and a cross-interrogate signal is transmitted to the instruction cache, and
>
> an operand store is allowed once exclusive status is obtained via the storage controller following a response from the cross interrogation."
>
> "Anderson also teaches that the cache coherency protocol (i.e.

interlocking mechanism) ensures that a processor accesses the most current data (Column 3, lines 3 7-44)."

"Regarding claims 24-26 and 28-30, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the cache coherency protocol enumerated above and taught by Anderson, in the system made obvious by the combination of Gaskins, Anderson and Handy as applied to claim 22 above, in order to ensure that a processor accesses the most current data as taught by Anderson."

"Gaskins, Anderson and Handy do not teach the following steps as required by claims 24-26 and 28-30, however, these steps are taught by Mahalingaiah:

buffering cache block addresses in a register-file (Fig. 2, element 48) in an instruction cache (Figs. 1 and 2, element 22) corresponding to fetched unexecuted instructions in an instruction buffer in the instruction unit (Column 3, lines 1-7; column 8, lines 34-37);

discarding and refetching data in the instruction cache if the associated cache block in the instruction cache matches the desired storage address (Column 3, lines 8-12; column 8, lines 41-59);

discarding and refetching data in the instruction buffer and re-buffering cache locations in the register if an instruction stream of an execution unit (Fig. 1, element 28) changes (i.e. if the code is self-modified, see Instant Application, page 6, lines 22-24) (Column 5, lines 13-29 and 54-58; column 8, lines 41-59; column 9, lines 48-60); and

discarding data in the instruction buffer and discarding the cache locations in the register if the execution unit completes execution of fetched instructions (Column 4, lines 13-15; column 8, lines 41-59)."

"Mahalingaiah teaches that the above steps allow correct execution of self-modifying code (Column 3, lines 12-14; column 5, lines 54-58)."

"Regarding claims 24-26 and 28-30, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the teachings of Mahalingaiah enumerated above, in the system made obvious by the combination of Gaskins, Anderson and Handy, in order to allow correct execution of self-modifying code as taught by Mahalingaiah."

"The rationale derived from Anderson in the rejection of claim 7 above is incorporated herein for the teaching required by claim 26 that when exclusive ownership of a cache block is requested, all other copies whether exclusive or read-only are invalidated."

"The rationale derived from Anderson in the rejection of claims 11-12 above is incorporated herein for the teachings required by claims 29-30 that the cross-interrogation of the cache block address is accomplished via a

directory lookup in the storage control unit."

"Regarding claims 26 and 29-30, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the cache coherency protocol enumerated above and taught by Anderson, in the system made obvious by the combination of Gaskins, Anderson, Handy and Mahalingaiah as applied to claim 24 above, in order to ensure that a processor accesses the most current data as taught by Anderson."

"Regarding claim 30, although the combination of Gaskins, Anderson, Handy and Mahalingaiah does not teach that the cache directory and register-file comprise six locations, such limitations are merely a matter of design choice and would have been obvious in the system of Gaskins, Anderson, Handy and Mahalingaiah. The combination of Gaskins, Anderson, Handy and Mahalingaiah teaches both a directory and register file. The limitations in claim 30 of the instant application do not define a patentably distinct invention since both are directed toward providing storage for indexing cache contents and instruction fetch unit contents. The number of locations is inconsequential for the invention as a whole and presents no new or unexpected result. Therefore, to use six locations would have been an obvious design choice to one of ordinary skill in the art at the time of invention by applicant."

With regard to Claims 24-26 and 28-30, Applicants respectfully contends that neither Gaskins, nor Anderson, nor Handy, nor Mahalingaiah, whether alone or in combination, teach or disclose each element of the invention as discussed above. Specifically, neither Gaskins, nor Anderson, nor Handy, nor Mahalingaiah, teach or disclose, "a storage controller", or "said central processing unit coupled to said storage controller". Applicants respectfully submit, that the Examiner suggests that the storage controller is internal to the CPU and comprised of the three elements of 620, 640, and 642, this clearly is not equivalent to the claim terminology as presented above. Moreover, neither Gaskins, nor Anderson, nor Handy, nor Mahalingaiah, teach or disclose, "a processor system with a storage controller and a central processing unit including an execution unit, an instruction unit, and a plurality of caches **including separate instruction cache and operand cache**" as discussed above. Therefore, because neither Gaskins, nor Anderson, nor Handy, nor Mahalingaiah, disclose or teach an element of the invention they cannot render the Applicants' claims unpatentable. Thus, Claims 24-26 and

28-30 are allowable, the rejections are improper, and they should be withdrawn.

Alternatively, assuming for the sake of argument, that the cited references are applicable, Applicant respectfully maintains that the Examiner has used an improper standard in arriving at the rejection of the above claims under section 103, by failing to provide any motivation for the suggested combination. "(E)ven assuming that all elements of an invention are disclosed in the prior art, an Examiner cannot establish obviousness by locating references that describe various aspects of a patent applicant's invention without also providing evidence of the motivating force which would have impelled one skilled in the art to do what the patent applicant has done." *Ex parte Levengood*, 28 U.S.P.Q. 1300 (Bd. Pat. App. Int. 1993). The references, when viewed by themselves and not in retrospect, must suggest the invention. *In Re Skoll*, 187 U.S.P.Q. 481 (C.C.P.A. 1975).

The explanation provided in the Office Action in this instance provides no justification or explanation for the suggested combination of the cited references, particularly Gaskins and Anderson. The rejection based on the suggested combination of references merely amounts to a compilation of the claimed elements without any suggestion or motivation for their combination. There are no teachings in the art or the cited references that would have motivated one skilled in the art to make the suggested combination. Therefore, the Examiner has not made a prima facie case for obviousness under §103(a). Thus, Claims 5 - 7, 9 –12, 19 - 26 and 28 - 33 are allowable, the rejections are improper, and they should be withdrawn.

Moreover, Applicant respectfully maintains that the Examiner has used an improper standard in arriving at the rejection of the above claims under section 103, based on improper hindsight which fails to consider the totality of Applicant's invention and to the totality of the cited references. More specifically, the Examiner has used Applicants' disclosure to select portions of the cited references to allegedly arrive at Applicants' invention. In doing so, the Examiner has failed to consider the teachings of the reference or Applicants' invention as a whole in contravention of section 103.

The amendments and arguments presented herein are made for the purposes of better defining the invention, rather than to overcome the rejections for patentability. The claims have not been amended to overcome the prior art and therefore, no presumption should attach that either the claims have been narrowed over those earlier presented, or that subject matter or equivalents thereof to which the Applicants are entitled has been surrendered. It is believed that the foregoing remarks are fully responsive to the Office Action and that the claims herein should be allowable to the Applicants. Accordingly, reconsideration of the claims and withdrawal of the rejections are requested.

In the event the Examiner has any queries regarding the instantly submitted response, the undersigned respectfully requests the courtesy of a telephone conference to discuss any matters in need of attention.

If there are additional charges with respect to this matter or otherwise, please charge them to Deposit Account No. 06-1130.

Respectfully Submitted,

CANTOR COLBURN LLP

By _____

Troy J. LaMontagne
Registration No. 47,239
55 Griffin Road South
Bloomfield, CT 06002
Telephone: (860) 286-2929
Facsimile: (860) 286-0115

Date: January 23, 2004